Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **17EC3042** | **Duration :** | **3hrs** |
| **Sub. Name :** | **SYSTEM ON CHIP DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Calculate the buffers required , optimal buffer size, 50% delay when a minimum size inverter drives a metal 1 wire that is 2000λ X 3 λ. R0 = 5.0 Kᾩ and C0 =0.69 fF while Rint = 58 ᾩ and Cint= 106 fF. | CO1 | 10 |
| b. | Sketch the stick diagrams of 3 input NAND gate. | CO1 | 5 |
| c. | Sketch the 3 input domino NAND gate and explain its operation. Discuss capacitive coupling and charge sharing in domino circuits. | CO1 | 5 |
| (OR) | | | | |
| 2. | a. | Analyze the delay through inductive interconnect with suitable diagrams. | CO1 | 12 |
| b. | Sketch the 2 input pseudo –nMOS NOR transistor and explain its operation. Determine the relationship between the W/L ratios of the pullup and the pulldown transistors to provide reasonable output voltages for the gate. | CO1 | 8 |
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| 3. | a. | Evaluate the logical effort of a given function assuming r= 2  . | CO2 | 8 |
| b. | Illustrate combinational network delay with examples. | CO2 | 12 |
| (OR) | | | | |
| 4. | a. | Consider a chain of four, 4 - input NAND gates. The first NAND gate is driven by a minimum-size inverter and the output of the last NAND gate is connected to an inverter that is 6X the minimum size. Calculate the path effort (F) , optimum effort per stage and output-to-input capacitance ratio. | CO2 | 12 |
| b. | Describe cross-talk minimization in wires with an example. | CO2 | 8 |
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| 5. | a. | Design a traffic light controller using FSM. Write a Verilog code to implement it FPGA. | CO6 | 15 |
| b. | Analyze the performance of latch based machines with suitable diagram | CO2 | 5 |
| (OR) | | | | |
| 6. | a. | Construct latch and flip-flop using transmission gates and explain their operation. | CO2 | 10 |
| b. | Construct the state transition table for a four- bit shift register. | CO2 | 10 |
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| 7. | a. | Write a Verilog code to construct a 4-bit carry lookahead adder. | CO6 | 10 |
| b. | Sketch the structure of a 4-bit Wallace tree multiplier and explain its operation. | CO6 | 10 |
| (OR) | | | | |
| 8. | a. | Evaluate (14) x (-12) using Booth algorithm. | CO6 | 10 |
| b. | Implement the given function in PAL structure of an Altera device.  F = A' · C · D + B' · C · D + A · B + B · C' | CO6 | 10 |
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|  | | **Compulsory**: |  |  |
| 9. | a. | Point-out the goals and objectives of global routing and detailed routing. | CO3 | 6 |
| b. | Compare Lee maze-running algorithm with line -probe algorithm for detailed routing. | CO3 | 14 |